In the claims:

1. – 6. (canceled)

8. (currently amended) An ethernet switch assembly comprising:

a multiple port crossbar switch including first, second, and third crossbars, each of said first, second, and third crossbars including M ports and a switch matrix capable of switching ethernet data from one of its ports to another of its ports, and a plurality of interconnect buses, a first set of K ports of said first crossbar coupled to a first set of K ports of said second crossbar through K of said interconnect buses, a second set of K ports of said first crossbar coupled to a first set of K ports of said third crossbar through K of said interconnect buses, and a second set of K ports of said second crossbar coupled to a second set of K ports of said third crossbar through K of said interconnect buses, wherein L ports of each of said first, second and third crossbars are available as ports for said multiple port crossbar switch, and wherein $M > L > K$, and $(3xL)>M$, so that the number of external ports of the multiple port crossbar switch is increased beyond the number of ports of each of the first, second, and third crossbars; and

a plurality of ethernet controllers each having a first input coupled to a respective one of said available ports of said multiple port crossbar switch via an interconnect bus.

9. (original) The ethernet switch assembly of Claim 8, wherein $M = 12$, $L = 6$ and $K = 3$.

10. (original) The ethernet switch assembly of Claim 8, wherein each of said plurality of ethernet controllers further have an output coupled to a PHY communication layer.

11. (original) The ethernet switch assembly of Claim 8, wherein one of said interconnect buses comprises a full duplex bus operating at approximately 2.88 Gigabits/second.

12. (original) The ethernet switch assembly of Claim 8, wherein each of said first, second and third crossbars is a 12-port crossbar chip.

13. (original) The ethernet switch assembly of Claim 8, wherein one of said interconnect buses is a chip-to-chip bus operating at 2.88 Gigabits/second full duplex.

14. (original) The ethernet switch assembly of Claim 8, wherein each of said interconnect buses is a chip-to-chip interconnect bus.

15. (original) The ethernet switch assembly of Claim 8, wherein each of said interconnect buses coupling said crossbars is a chip-to-chip interconnect bus.

16.- 19. (canceled)